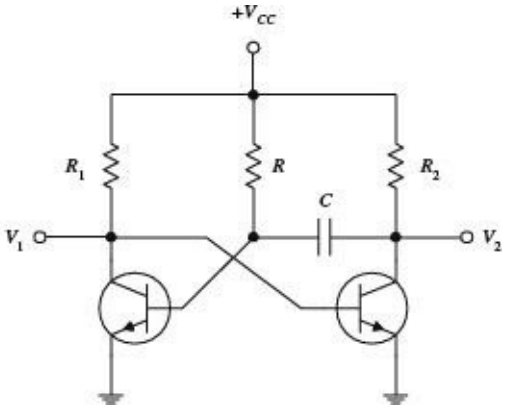
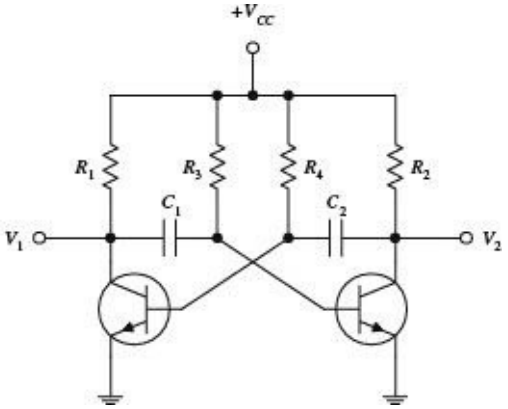


MONOSTABLE MULTIVIBRATOR (2D CIRCUIT) A monostable multivibrator is a circuit that is stable in only one state. It can be thrown into its unstable state by applying an external signal, but it will automatically return to its unstable state afterward. When V_1 = 0 V, the circuit is in its stable state. However, if you momentarily ground V_2, the capacitor suddenly behaves like a short circuit (a capacitor likes to pass current when the voltage across it changes suddenly) and causes the base current and hence the collector current of the left-hand transistor to go to zero. Then, all the current through R_1 flows into the base of the right-hand transistor, holding it in its saturation state until the capacitor can recharge through R. This in turn causes the circuit to switch back to its initial state. This kind of circuit produces a square pulse of voltage at V_1 with a duration determined by the RC time constant and which is independent of the duration and amplitude of the pulse that caused it to change states.



ASTABLE MULTIVIBRATOR (3D CIRCUIT) This circuit is not stable in either state and will spontaneously switch back and forth at a prescribed rate, even when no input signals are present. To understand how this circuit works, initially assume that V_1 is grounded. This means that the base of the right-hand transistor also will be at ground, at least until C_1 can charge up through R_2 to a high enough voltage to cause the right-hand transistor to saturate. At this time, V_2 then goes to zero, causing the base of the left-hand transistor to go to zero. V_1 then rises to a positive value, at least until C_2 can charge up through R_4 to a high enough voltage to cause the left-hand transistor to saturate. The cycle repeats itself over and over again. The time spent in each state can be controlled by the R_C networks in the base section (R_3C_1 and R_4C_2 time constants set the time duration). As you can see, an astable multivibrator is basically a simple oscillator with an adjustable wave pattern (time spent in each state).

FIGURE 4.68

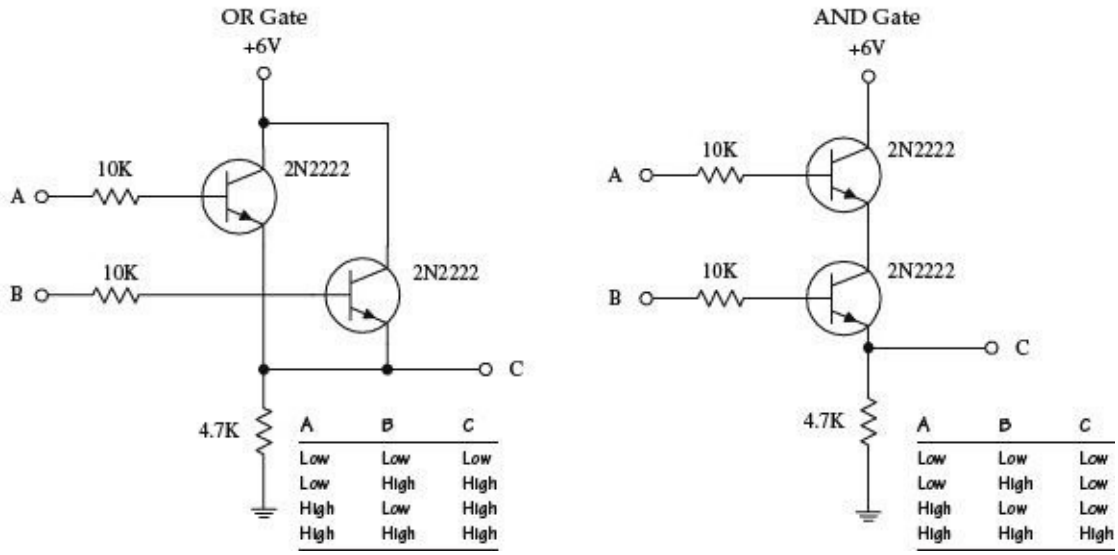


FIGURE 4.69 The two circuits here form logic gates. The OR circuit allows the output (*C*) to swing to a high voltage when either *A* or *B* or both *A* and *B* are high. In other words, as long as at least one of the transistors is biased (turned on), a high voltage will appear at the output. In the AND gate circuit, both *A* and *B* must be high in order for *C* to go high. In other words, both transistors must be biased (turned on) for a high voltage to appear at the output.

4.3.3 Junction Field-Effect Transistors

Junction field-effect transistors (JFETs) are three-lead semiconductive devices that are used as electrically controlled switches, amplifier controls, and voltage-controlled resistors. Unlike bipolar transistors, JFETs are exclusively voltage-controlled—they do not require a biasing current. Another unique trait of a JFET is that it is normally on when there is no voltage difference between its gate and source leads. However, if a voltage difference forms between these leads, the JFET becomes more resistive to current flow (less current will flow through the drain-source leads). For this reason, JFETs are referred to as *depletion devices*, unlike bipolar transistors, which are en-hancement devices (bipolar transistors become less resistive when a current/voltage is applied to their base leads).

JFETs come in either *n-channel* or *p*-channel configurations. With an n-channel JFET, a negative voltage applied to its gate (relative to its source lead) reduces current flow from its drain to source lead. (It operates with $V_C > V_S$.) With a *p*-channel JFET, a positive voltage applied to its gate reduces current flow from its source to drain lead. (It operates with $V_S > V_C$.) The symbols for both types of JFETs are shown below.

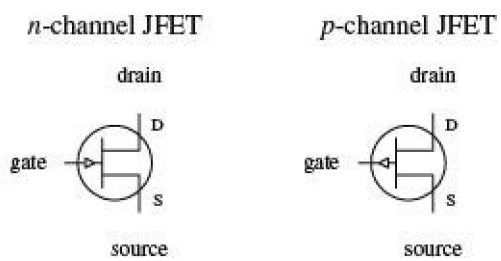


FIGURE 4.70

An important characteristic of a JFET that is useful in terms of applications is its extremely large input impedance (typically around 10^{10} Ω). This high input impedance means that the JFET draws little or no input current (lower pA range) and there-fore has little or no effect on external components or circuits connected to its gate—no current is drawn away from the control circuit, and no unwanted current enters the control circuit. The ability for a JFET to control current flow while maintaining an extremely high input impedance makes it a useful device used in the construction of bidirectional